

## **REMARKS/ARGUMENTS**

### **Specification**

In the specification, various paragraphs have been amended to make typographical changes and/or to provide consistency between reference numbers in the text and the Figures.

### **Figures**

Nineteen (19) sheets of formal drawings are submitted herewith along with a corresponding Letter To Official Draftsperson.

### **Claims**

Claims 1 through 11 were in this application and addressed by the Examiner in the present 13, 2003 Office Action. The present Amendment amends claims 1 through 4, 7, 8, and 10. The rejection and amendments to the claims are addressed below.

### **Claim Objections**

Claim 3 is objected to for the informality of missing a final period at the end of the claim. Claim 3 is amended herein to add that period.

### **Rejections Under 35 U.S.C. § 112**

Claims 1 through 12 are rejected under 35 U.S.C. § 112, second paragraph.

Claim 1 is rejected in this regard for lack of antecedent basis for the limitation "each data access instruction". This limitation is amended to recite, "coding a plurality of data access instructions of the algorithm module . . ." and, thus, the rejection is overcome. Claim 7 is similarly rejected and similarly amended.

Claim 2 is rejected in this regard as the Examiner found it unclear as to what was being prohibited from direct access. Claim 2 is amended to recite, "prohibiting the algorithm module from direct access to a peripheral device." Antecedent support for this amendment may be found, by way of example, in the specification at page 19, lines 18 through 20.

Claim 2 is further rejected in this regard for lack of antecedent basis for the limitation "each algorithm header." This limitation is amended to recite, "naming an algorithm header of the algorithm module . . ." and, thus, the rejection is overcome.

Claim 2 is further rejected in this regard for lack of antecedent basis for the limitation "all external identifiers." This limitation is amended to recite, "naming each

external identifier, in a set of external identifiers defined by the algorithm module, . . . and, thus, the rejection is overcome.

Claim 8 is similarly rejected on the bases of claim 2 and is similarly amended.

Rejections Under 35 U.S.C. § 103(a)

Claim 1 is rejected under 35 U.S.C. § 103(a) over Every in view of Ganssle and Kogure. However, the Examiner then singularly identifies limitations of each of these references in what they fail to teach as to the claimed invention, as a whole. For example, the Examiner asserts that Every teaches one aspect, but does not teach others. Then, the Examiner turns to Ganssle to teach another aspect, yet then acknowledges that neither Every nor Ganssle teaches additional aspects, then turning to Kogure. Applicants respectfully submit that there is no suggestion in the cited references to combine them in this way. Instead, the Examiner is possibly using the benefit of hindsight to collect these references. Further, there is no suggestion in certain instances as to applying the cited references to the context of claim 1. For example, claim 1 recites, "[a] method for creating an algorithm module that can be used without change in a plurality of frameworks." Every, by way of example, is nothing more than an explanation of reentrancy. It in no way points itself to the recited context and use of claim 1. Similar observations may be made with respect to Ganssle, which is directed to an explanation of relocatable code.

Lastly with respect to Claim 1, while Kogure includes aspects related to static and dynamic memory allocation, that patent does not describe, as in claim 1, the manner of removing the function of instantiation to a framework, and where that framework may be "any framework in [a] plurality of frameworks." Indeed, the present Specification contrasts prior art memory management with that of the invention, by way of example at page 13, lines 15 through 20, as follows:

"It has now been discovered that several technical issues have prevented the creation of such a method. One major issue is that algorithm implementations to date have been responsible for managing their own memory usage. If an algorithm is to be used in a variety of applications, the framework rather than the algorithm must make decisions about memory usage and preemption."

The operation of the framework in this respect appears in amended claim 1, and is not in any way shown by the Kogure (or other cited) references.

For any of the preceding reasons, therefore, Applicants respectfully submit that claim 1 and its dependent claims 2 through 6 are in condition for allowance. In addition,

independent claim 7 is similarly amended and, thus, it and its dependent claims 8 through 11 are also in condition for allowance.

In addition to the preceding, the Examiner appears to have not read, in view of the Specification, an aspect of claims 2 and 8 as directed to the step of "characterizing a ROM-ability mode of in the algorithm module." Specifically, the Examiner cites to Hosotani in this regard and states that it teaches "characterizing a program's ability to be altered in ROM, by means of a flag." However, Applicants had previously defined their intended scope, as their own lexicographer, of the recitation pertaining to ROM-ability, in the Specification by way of example at page 19, lines 16 and 17, which state:

"Algorithms must characterize their ROM-ability; i.e., state whether they may be placed in ROM or not.

Applicants respectfully submit, therefore, that this aspect differs from that cited by the Examiner and, thus, is not shown in the cited reference. Moreover, to ensure observation of this point, the present amendment adds this language into claims 2 and 8 so that each is consistent with the previously-existing definition as intended, namely, both claims now include the step of "characterizing in the algorithm module whether the algorithm module may or may not be placed in ROM;" Thus, in addition to the reasons set forth above, claims 2 and 8, as well as the claims depending from them, are in condition for allowance.

#### Information Disclosure Statement

An Information Disclosure Statement is filed herewith, making of record the references cited in the two related cases identified at the beginning of the Specification.

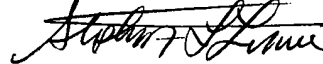
#### Fees and Extension Of Time

A Petition for a One (1) month of extension of time is submitted herewith, along with a Fee Sheet authorizing payment for said Extension and also for the additional claims added in this amendment. The Fee Sheet also authorizes payment for the fee for the Information Disclosure Statement.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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The undersigned hereby certifies that this correspondence is being deposited with the U.S. Postal Service, as first class mail, on the following date and to the addressee listed below

**Mailed: March 5, 2004.**

To: Commissioner for Patents  
P.O. Box 1450  
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